**Homework 3**

**Problem Statement:**

**In this assignment, you are to design a circuit that has two input ports: data (8-bit) and reset (1-bit) and one 4-bit output port. After a complete synchronous pulse on reset, in the next eight clocks, the circuit receives eight bytes of data on the data port on every rising edge of clock. There is a module which calculates number of 1s for each received input. The output of this circuit should be maximum number of 1s between all 8 inputs (As the maximum value of output is 8, 4 bits is enough for it).**

Flow Diagram:



State Diagram:

Code:

library ieee;

use ieee.std\_logic\_1164.all;

entity and\_gate is

port (

in1, in2 : in std\_logic;

or\_out : out std\_logic

);

end entity and\_gate;

architecture and\_arch of and\_gate is

begin

process (<>)

begin

end process;

end <>;

library ieee;

use ieee.std\_logic\_1164.all;

entity bin\_adder is

port (

A, B : in std\_logic\_vector (3 DOWNTO 0);

AplusB : out std\_logic\_vector (3 DOWNTO 0)

);

end entity bin\_adder;

architecture <> of <> is

begin

process (<>)

begin

end process;

end <>;

library ieee;

use ieee.std\_logic\_1164.all;

entity demux8to4 is

port (

in8 : in std\_logic\_vector (7 DOWNTO 0);

out4 : out std\_logic\_vector (3 DOWNTO 0)

);

end entity demux8to4;

library ieee;

use ieee.std\_logic\_1164.all;

entity delay1 is

port (

D, clk : in std\_logic;

D\_out : out std\_logic

);

end entity delay1;

architecture <> of <> is

begin

process (<>)

begin

end process;

end <>;

library ieee;

use ieee.std\_logic\_1164.all;

entity counter4bit is

port (

in3 : in std\_logic;

clk : in std\_logic;

counter\_out : out std\_logic\_vector (3 DOWNTO 0)

);

end entity counter4bit;

architecture <> of <> is

begin

process (<>)

begin

end process;

end <>;